

WHAT IS CLAIMED IS:

1. A capacitor for an integrated circuit comprising:
  - a first MOS-on-NWELL device formed on a substrate and having a first pickup terminal and a first gate;
  - a second MOS-on-NWELL device formed on the substrate and having a second pickup terminal and a second gate,
  - wherein the first gate is connected to the second pickup terminal, and
  - wherein the second gate is connected to the first pickup terminal.
2. The capacitor of claim 1, further comprising:
  - a first PMOS transistor formed on the substrate and having its source and drain terminals connected together; and
  - a second PMOS transistor formed on the substrate and having its source and drain terminals connected together,
  - wherein a gate of the first PMOS transistor is connected to the source and drain terminals of the second PMOS transistor,
  - wherein a gate of the second PMOS transistor is connected to the source and drain terminals of the first PMOS transistor, and
  - wherein a combination of the first and second PMOS transistors are connected in parallel with the first and second MOS-on-NWELL devices.
3. A capacitor for an integrated circuit comprising:
  - a first PMOS transistor formed on a substrate and having its source and drain terminals connected together;
  - a second PMOS transistor formed on the substrate and having its source and drain terminals connected together,
  - wherein a gate of the first PMOS transistor is connected to the source and drain terminals of the second PMOS transistor, and
  - wherein a gate of the second PMOS transistor is connected to the source and drain terminals of the first PMOS transistor.

4. The capacitor of claim 3, further comprising:
  - a first MOS-on-NWELL device formed on the substrate and having a first pickup terminal and a first gate;
  - a second MOS-on-NWELL device formed on the substrate and having a second pickup terminal and a second gate,
  - wherein the first gate is connected to the second pickup terminal, and
  - wherein the second gate is connected to the first pickup terminal, and
  - wherein a combination of the first and second PMOS transistors are connected in parallel with the first and second MOS-on-NWELL devices.
5. A capacitor for an integrated circuit comprising:
  - a first plurality of MOS-on-NWELL devices connected between a positive and a negative voltage to operate in an accumulation region as capacitors;
  - a second plurality of MOS-on-NWELL devices connected between the positive and the negative voltage to operate in a depletion region as capacitors;
  - a first plurality of PMOS transistors connected between the positive and the negative voltage to operate in an accumulation region as capacitors; and
  - a second plurality of PMOS transistors connected between the positive and the negative voltage to operate in a depletion region as capacitors.
6. A capacitor for an integrated circuit comprising:
  - a first MOS-on-PWELL device formed on a substrate and having a first pickup terminal and a first gate;
  - a second MOS-on-PWELL device formed on the substrate and having a second pickup terminal and a second gate,
  - wherein the first gate is connected to the second pickup terminal, and
  - wherein the second gate is connected to the first pickup terminal.
7. The capacitor of claim 1, further comprising:

a first NMOS transistor formed on the substrate and having its source and drain terminals connected together; and

a second NMOS transistor formed on the substrate and having its source and drain terminals connected together,

wherein a gate of the first NMOS transistor is connected to the source and drain terminals of the second NMOS transistor,

wherein a gate of the second NMOS transistor is connected to the source and drain terminals of the first NMOS transistor, and

wherein a combination of the first and second NMOS transistors are connected in parallel with the first and second MOS-on-PWELL devices.

8. A capacitor for an integrated circuit comprising:

a first NMOS transistor formed on a substrate and having its source and drain terminals connected together;

a second NMOS transistor formed on the substrate and having its source and drain terminals connected together,

wherein a gate of the first NMOS transistor is connected to the source and drain terminals of the second NMOS transistor, and

wherein a gate of the second NMOS transistor is connected to the source and drain terminals of the first NMOS transistor.

9. The capacitor of claim 3, further comprising:

a first MOS-on-PWELL device formed on the substrate and having a first pickup terminal and a first gate;

a second MOS-on-PWELL device formed on the substrate and having a second pickup terminal and a second gate,

wherein the first gate is connected to the second pickup terminal, and

wherein the second gate is connected to the first pickup terminal, and

wherein a combination of the first and second NMOS transistors are connected in parallel with the first and second MOS-on-PWELL devices.

10. A capacitor for an integrated circuit comprising:
  - a first plurality of MOS-on-PWELL devices connected between a positive and a negative voltage to operate in an accumulation region as capacitors;
  - a second plurality of MOS-on-PWELL devices connected between the positive and the negative voltage to operate in a depletion region as capacitors;
  - a first plurality of NMOS transistors connected between the positive and the negative voltage to operate in an accumulation region as capacitors; and
  - a second plurality of NMOS transistors connected between the positive and the negative voltage to operate in a depletion region as capacitors.